A Novel Common-Mode Noise Reduction Using Hybrid Balance Method Applied to Single Switch Converter

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Abstract

A typical single-phase switching converter inherently has unbalanced characteristics due to the DC source, transmission path (TP), and load terminals. Because of the unbalance, there exists a common mode (CM) noise current, which flows into the frame ground (FG). This paper presents the hybrid balance (active plus passive balance) technique to improve the system unbalance situation applied to a single-switch converter by using two-switching (active balance) converters to balance TP and the passive balance (compensated capacitors) scheme for the DC source and load. The reduction mechanism of the CM noise is explained using the equivalent circuit model. The improvement is achieved utilizing the hybrid balancing technique and the results are validated based on the CM rejection ratio (CMRR). The experimental results have shown that the hybrid balance technique can improve the conducted CM noise reduction by 36.07 dB.

Keywords

EMI, Switching noise, noise suppression, unbalance converter, CMRR

1. Introduction

In a multi-wire electrical system, the current can be decomposed into a differential mode (out-of-phase) current and common mode (in-phase) current. Between the two current types with equal amplitude, the common mode (CM) current emanates a stronger EM interference (EMI) field due to the current in-phase nature, and it must be controlled for emission reduction. On the other hand, the field emanating from the differential mode (DM) current is normally less than CM field due to its cancellation nature. To reduce the CM current of a system, the circuits have to be balanced with respect to FG.

In the single-phase MOSFET switching converter (Q_1) for DC motor speed control application, there are several components that influence the impedance unbalance with respect to FG, such as, DC source, load, and

transmission paths (TP). The 36V DC source and the load as shown in Fig. 1(a) exhibit an inherent imbalance. For the multi-wire system, the TP impedance is also unbalanced especially due to the switching action time delay of Q_1. As the result, there exists the CM current, which is an unwanted current. In an attempt to find an applicable solution to combat the conductive CM noise, several existing approaches such as CM choke filters, snubber circuit and anti-phase winding portions are evaluated for their performance.

The CM choke is mostly used to suppress the conductive CM noise. The shortcomings are associated with the cost, size, weight, insertion loss [1-2] and the magnification of noise at the series resonance frequencies [3]. The snubber circuit is used to reduce dv/dt and di/dt by transferring the switching energy from the active switch to the energy storage element (capacitor). This circuit suffers the same drawback similar to CM chock [4-5]. An anti-phase winding [6] or the passive cancellation method [7] is based on the generation of an out-of-phase current to the CM current at only one node section, with no consideration to the entire circuit system. Recently, the balanced switching converter has been presented [8-9]. The method deals with only the passive balance compensation and is limited to balancing only the TP connection between the DC source and load. However, this method does not address the remaining imbalance issues of the circuit system.

This paper proposes the hybrid-balance scheme to overcome the circuit system unbalance. Two active MOSFET switches (Q_1 and Q_2) will active balance the TP section and compensated capacitors in center-tap-configuration for the unbalanced DC source and load sections. To evaluate the performance of the scheme, the CM rejection ratio (CMRR) is used. Finally, the effectiveness of the proposed conductive CM noise reduction method is demonstrated via numerous experiments.

2. Unbalanced circuit of a single MOSFET converter

The three aforementioned unbalanced characteristics existed in the single-switch converter system and are shown in Fig. 1(a). In order to determine the CM noise behavior and search for a practical solution to improve the impedance imbalance, the equivalent circuit shown in Fig. 1(b) is utilized. The TP imbalance is severely affected when the impedance of active switch is changing with the pulse width modulation (PWM) frequency, and is causing the sending path impedance with respect to the FG to fluctuate, and at the same time, the

impedance of the return path (Z_{TP}) is almost constant.

The DC source imbalance is due to the amplitude $|V_{AC}| > |V_{BC}|$ and is compounded further with

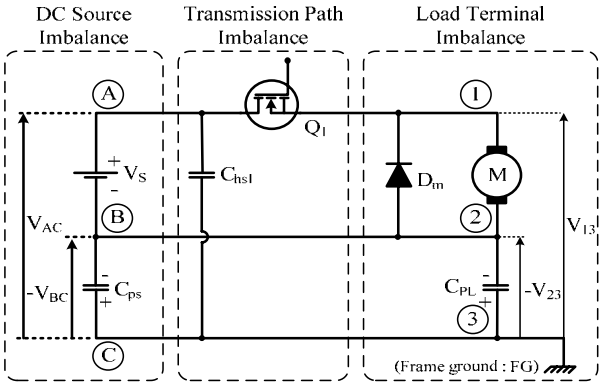
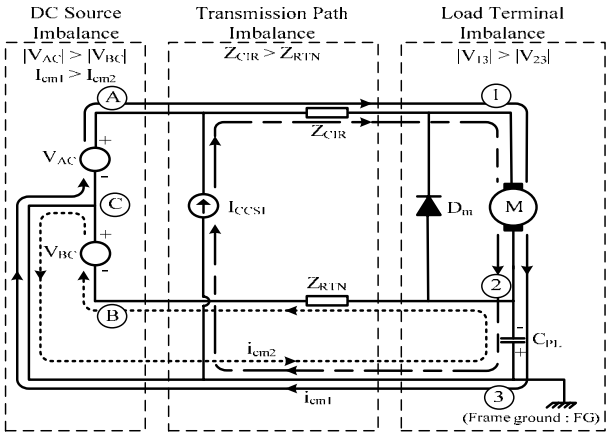


Figure 1(*a*). A single-switch converter



$$Z_{CIR} = Z_O^2/\Delta Z + Z_{TP}, Z_{RTN} = Z_{TP}$$

Figure 1(*b*). The equivalent circuit of the converter

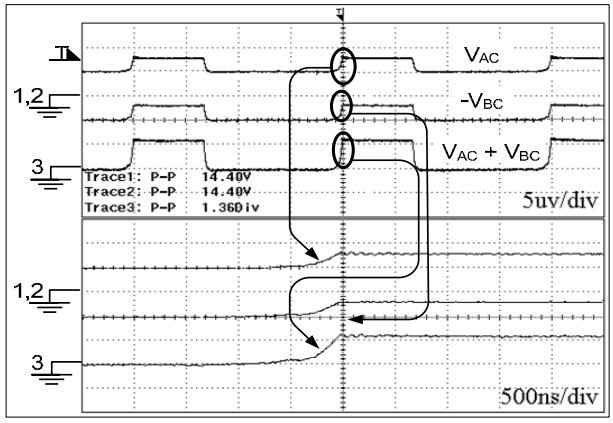


Figure 2.The measured waveforms of single-switch converter at the DC source terminal

the parasitic capacitance (C_{PS}). To illustrate the effects, V_{AC}, $-V_{BC}$ and the summation ($V_{AC} + V_{BC}$) are measured and depicted in Fig. 2. The vertical scale is set to 10V/div and 5μs/div for time scale. For clarity, the zoom (500ns/div time scale) proximal to the leading edge is plotted in the figure as well. The effect at the trailing edge is also investigated with a like result. Therefore, only the result of the rising edge is presented. Similar to the source, the load unbalance impedance happens because the amplitude $|V_{13}| > |V_{23}|$ and with the parasitic capacitance (C_{PL}) in addition. The C_{PS} and C_{PL} are the capacitive couplings between the circuit ground and FG at the source and load, respectively.

2.1.The effect of unbalance transmission path (TP)

The sending path CM current of Q_1 flows through the load and returns back via FG to the source, as shown in Fig. 1(b). The transition

impedance (ΔZ) of the active switch (Q_1) in the sending path can be described in the following equations,

$$\Delta Z = \frac{dV_{ds}/dt}{dI_{ds}/dt}, \quad (1)$$

$$\frac{C}{L}\Delta Z = \frac{C}{L}\frac{dV_{ds}/dt}{dI_{ds}/dt} = I_{CCS1}/V_{sp}, \quad (2)$$

$$V_{SP} = \frac{\left(\sqrt{L/C}\right)^2}{\Delta Z} I_{CCS1} = \frac{Z_O^2}{\Delta Z} I_{CCS1}, \quad (3)$$

where

ΔZ = transition impedance of the switching action,

I_{CCS1} = common-mode noise current source generated by Q_1 including parasitic capacitance of heat sink,

V_{sp} = sending path spike voltage with respect to FG,

V_{ds} = voltage between drain and source of the MOSFET,

I_{ds} = current passing through drain and source of the MOSFET,

$Z_o = \sqrt{L/C}$ = characteristic impedance of the TP,

L = parasitic inductance in the sending path,

C = parasitic capacitance between the sending path and FG, such as C_{hs1}.

From Eq. (3), it can be seen that the TP unbalance caused by ΔZ will produce the CM current (I_{CCS1}) to flow through the load and to FG.

2.2. The effect of unbalance DC source

The unbalanced characteristic of DC source of the single-switch converter can be explained when $|V_{AC}| > |V_{BC}|$ as shown in Fig. 2. The unbalanced circuit of single-switch converter and DC source will produce CM current I_{cm1} and I_{cm2} (see Fig. 1(b)) from V_{AC} and $-V_{BC}$, respectively. I_{cm1} and I_{cm2} can be calculated from the following equations.

$$I_{cm1} = \frac{(Z_{CPL} + Z_{RTN})}{Z_C} V_{AC} - \frac{Z_{CPL}}{Z_C} V_{BC} + \frac{Z_D}{Z_C} I_{CCS1}, \quad (4)$$

$$I_{cm2} = \frac{Z_{CPL}}{Z_C} V_{AC} - \frac{(Z_{CPL}^2 + Z_C)}{Z_B Z_C} V_{BC} + \frac{Z_E}{Z_B Z_C} I_{CCS1}, \quad (5)$$

where

$Z_C = (Z_A Z_B - Z_{CPL}^2)$,

$Z_D = (Z_A Z_{CPL}^2 - Z_A Z_B)$,

$Z_E = (Z_A Z_{CPL}^2 + Z_{CPL} Z_C - Z_A Z_B Z_{CPL})$,

$Z_A = (Z_{CIR} + Z_m + Z_{CPL})$, and

$Z_B = (Z_{CPL} + Z_{RTN})$.

2.3. The effect of unbalanced load

The unbalanced characteristic of the load occurs when $|V_{13}| > |V_{23}|$ as shown in Fig. 3. From Fig. 1(b), V_{13} and $-V_{23}$ can be expressed as,

$$V_{13} = V_{AC} - Z_{CIR}(I_{cm1} + I_{CCS1}) \quad (6)$$

$$V_{23} = -V_{BC} + Z_{RTN} I_{cm2} \quad (7)$$

As V_{13} switches high $-V_{23}$ switches low. Hence $V_{13}+V_{23}$ varies from 0 to 16.8 V, as shown in Fig.3, trace 3. The CM voltage ($V_{13}+V_{23}$)

existed due to the load unbalance will degrade the circuit performance and the unit may fail the compliance for the EMI conducted emissions.

3. Balance transmission path (TP) using two MOSFET (Active balance) converters

The unbalanced TP can be improved by utilizing two MOSFET switches (Q1 and Q2) acting as the active balance converter, in which each switch is installed on the sending path as well as the return path, as shown in Fig. 4(a). The equivalent circuit model is shown in Fig. 4 (b). The Q_1 and Q_2 are driven by the synchronized PWM technique. From Fig. 4(b), when $I_{CCS1} = - I_{CCS2}$ and $Z_{CIR} = Z_{RTN}$, then the TP is in balance.

This is achievable if Q1 and Q2 are the same type and with proper selection of capacitors in TP section. However, this approach does not eliminate the DC source and load unbalances. In other words, $V_{AC} + V_{BC}$ or $V_{13} + V_{23}$ is not zero.

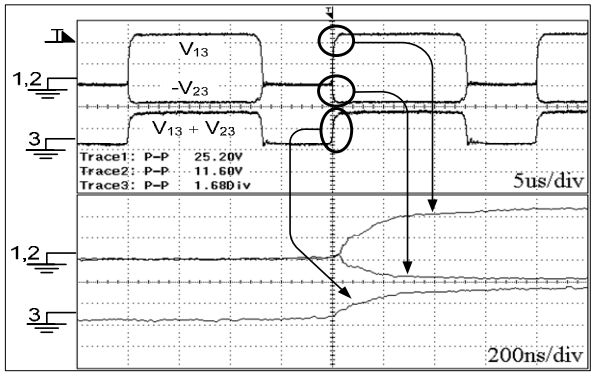


Figure 3.The measured waveforms of singleswitchconverterat the load terminal

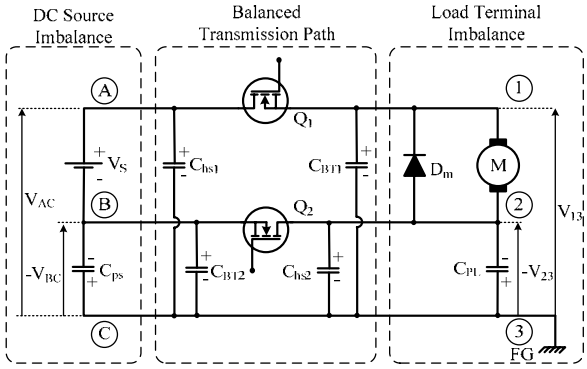


Figure 4(*a*). The two-switch converter

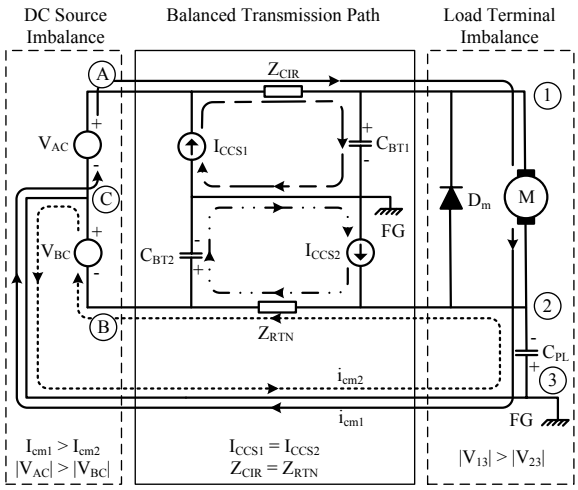


Figure 4(*b*). The equivalent circuit of the two-switch (active balance) converter

4. **Circuit balance using the hybrid balance**

For the converter, the entire circuit balance is possible with the use of two MOSFETs (active balance) and passive-balancing methods, herein is referred to as the hybrid-balancing scheme. The TP is balanced using Q_1 and Q_2, as shown in Fig. 5(a). Next, it is necessary to balance the DC source and load terminals by a passive balancing method, in which the capacitors in center-tap configuration (C_{S1} and C_{S2}) are introduced. The load-terminal balance is also realized by the simply connecting two capacitors (C_{BL1} and C_{BL2}), at the load terminals (1 and 2) to FG. The load balance will provide the symmetrical loop impedance or the loop component between the two loop CM currents of I_{cm1} and I_{cm2}. From Fig. 5(b), the entire circuit balance has been achieved using the proposed method. It can be seen that $|V_{AC}| = |V_{BC}| = V_s/2$. Also at FG, I_{cm1} and I_{cm2} flow in opposite directions, and therefore cancellation occurs.

The load-terminal balance can be described by the following equations:

$$V_{AC} - I_{cm1} Z_{CIR} - I_{CCS1} Z_{CIR} - V_{13} = 0,$$
$$V_{13} = V_S/2 - Z_{CIR}\left(I_{cm1} + I_{CCS1}\right), \quad (8)$$
$$-V_{BC} - V_{23} + I_{cm2} Z_{RTN} + I_{CCS2} Z_{RTN} = 0,$$
$$V_{23} = -V_S/2 + Z_{RTN}\left(I_{cm2} + I_{CCS2}\right), \quad (9)$$
$$\left.\begin{aligned} |V_{13}| &= |V_{23}| \\ V_{CM} &= V_{13} + V_{23} = 0 \end{aligned}\right\}, \quad (10)$$

Hence, it can be concluded that CM voltage (V_{CM}) is zero between the load terminals with respect to FG. To validate this finding, the measured waveforms at the DC source are shown in Fig. 6 where $V_{13} + V_{23}$ becomes zero. This is the desired result to minimize V_{CM}.

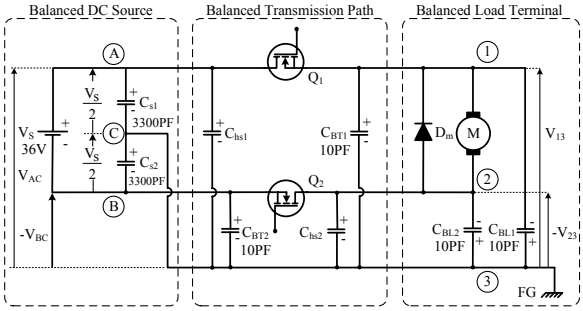


Figure 5(*a*). The hybrid balance scheme

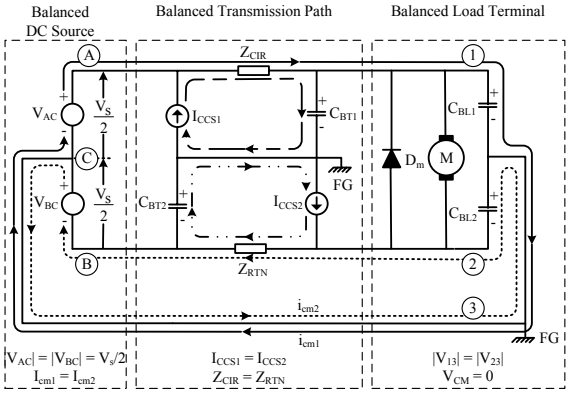


Figure 5(*b*). The equivalent circuit for the hybrid balance connection

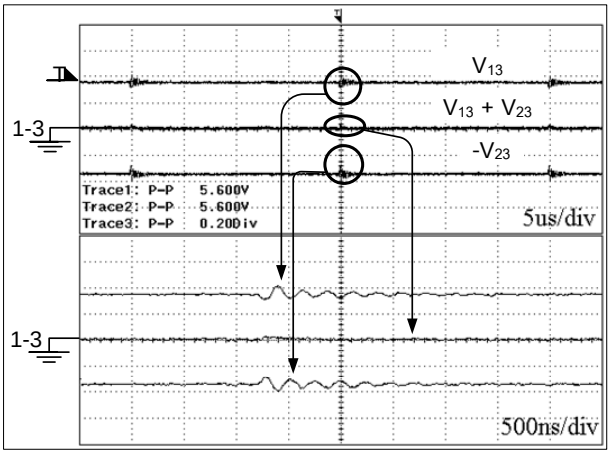


Figure 6. The waveforms using two-switch converter with passive balance at the DC source

Also, the CM currents, can be found as follows,

$$I_{cm1} = \left(V_S/2 - I_{CCS1}Z_{CIR}\right)/\left(Z_{CIR} + Z_{BL1}\right), \quad (11)$$

$$I_{cm2} = \left(V_S/2 - I_{CCS2}Z_{RTN}\right)/\left(Z_{RTN} + Z_{BL2}\right) \quad (12)$$

Here, I_{CSS1} = $-I_{CCS2}$, $Z_{CIR} = Z_{RTN}$, $Z_{BL1} = Z_{BL2}$.

Hence, $I_{cm1} = -I_{cm2}$, (13)

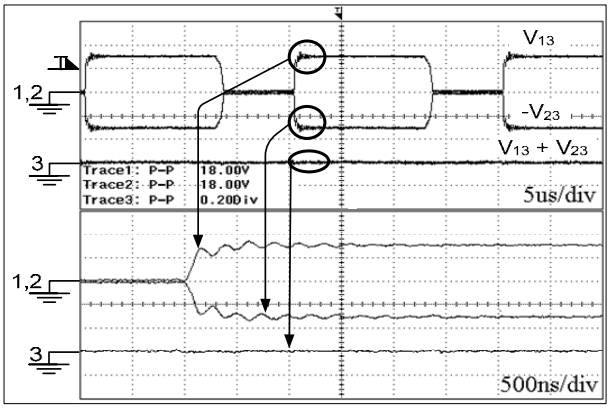


Figure 7. The waveforms using two-switch converter with passive balance at the load terminal

The measured waveforms of V_{13} and $-V_{23}$ and $V_{13} + V_{23}$ at the load are shown in Fig. 7. Again, despite the V_{13} and $-V_{23}$ fluctuations, the $V_{13} + V_{23}$ is still zero. Hence, the load impedance with respect to FG is in balance.

5. Evaluation of circuit balance by CMRR

The CM rejection ratio (CMRR) is used as an indicator of circuit balance [10]. The CMRR is defined as follows:

$$\mathrm{CMRR} = 20\log\frac{V_{DM}}{V_{CM}}, \quad (14)$$

$$\left.\begin{aligned} V_{DM} &= \left(V_{13} - V_{23}\right)/2 \\ V_{CM} &= V_{13} + V_{23} \end{aligned}\right\}, \quad (15)$$

Where V_{CM} = common-mode noise voltage, V_{DM} = differential mode noise voltage across load terminals.

The load-terminal voltages (V_{13} and $-V_{23}$) are measured and the CMRRs are calculated and summarized in Table 1 for three techniques. Also the improvement over the single-switch converter in dB is calculated. The two converters and the hybrid scheme provide reductions of 7.17 dB and 36.07 dB, respectively.

Table 1. The comparison by means of CMRR

Balance Scheme	(V_{DM}) (volt)	(V_{CM}) (volt)	CMRR (dB)	Improvement dB above single-switch converter
Single MOSFET converter	11.96	6.5	5.29	0
Two MOSFET converters	10.92	2.6	12.46	7.17
Two MOSFET converters with passive balance (Hybrid)	11.70	0.1	41.36	36.07

6. Stress voltage of the two-MOSFET converter technique

The double-switch scheme (Fig. 5(a)) does not only improve the path imbalance of the sending and returning paths, but also decrease the stress voltage over the single switch circuit (Fig. 1(a)) by two fold. With this advantage, the designer can select MOSFET having the rated voltage only half of the DC source. The switching power loss associated with Q_1 and Q_2 is

$$P_{diss} = (1/2)V_{ST}I_{SW}f_{SW}(T_{on} + T_{off}), \quad (16)$$

where V_{ST} = stress voltage of active switch,

I_{SW} = switching current,

f_{SW} = PWM frequency,

T_{on}, T_{off} = turn-on and turn-off time of active switch, respectively.

Since the stress voltage for each active switcher is half of the single switch scheme and I_{cm1} is equal to I_{cm2} (see Fig. 5(b)), then the switching power loss of the two switches is the same as the single switch and the measured data are demonstrated in Table 2., a Switching power loss comparison between the single-switch converter and that of the two-switch converter under the same input power and load conditions (V_S = 36 v, f_{SW} = 50 kHz, duty cycle = 65%, load (DC servo motor), I_{SW} = 200 mA.)

Table 2. A Switching power loss comparison between the single-switch and that of the two-switch converter

Typical of converter	V_{ST} (volt)	t_{on} (μsec)	t_{off} (μsec)	Switching power loss (watt)
Single-switch converter	36	0.66	0.805	0.2637 for one active switch
Two-switch converter	18	0.66	0.805	0.13185 for one active switch
				0.2637 for two active switches

7. Experimental results of the CM noise emissions

Fig. 8 is the experimental setup for this study. The line impedance stabilization network (LISN), spectrum analyzer and the current probe are the major equipment used during the experiment. The frequency spectrums of CM noise are measured and shown in Figs. 9-11 for the single switch converter, two-switch (active balance) converter, and two-switch converter with passive balance (hybrid balance), respectively. It can be seen from Fig. 9 that the single-switch converter has the highest noise. With two-switch (active balance) converter, the noise is reduced as compared to the former, on the average, about 10 dB (Fig. 10) for all frequency observed. The noise for hybrid technique is depicted in Fig. 11.

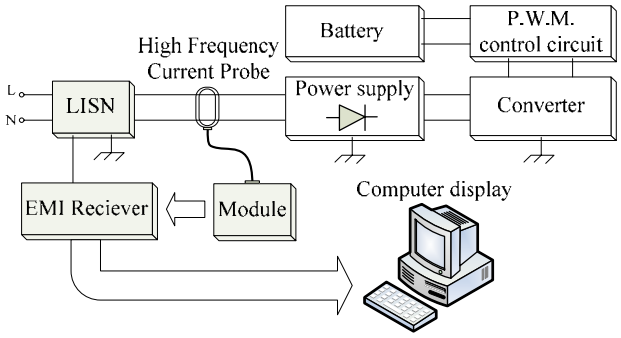


Figure 8. Experimental Setup for conductive CM noise measurement

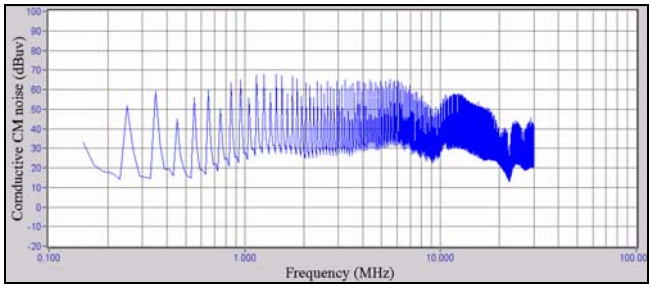


Figure 9. CM emissions of single-switch converter

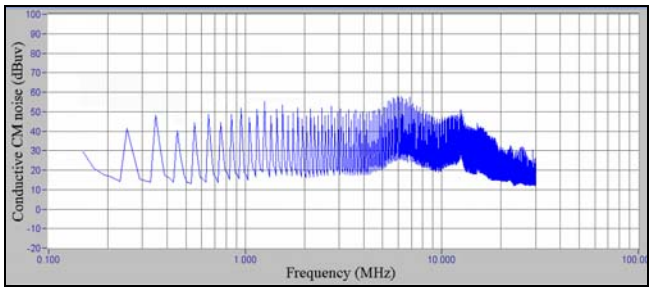


Figure 10. CM emissions of two-switch (active balance) converter

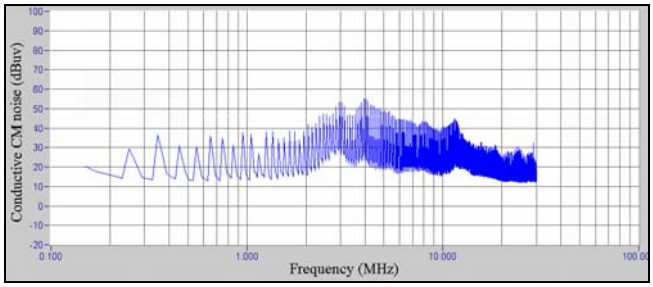


Figure 11. CM emission of the proposed hybrid scheme (two-MOSFET converter with passive balance)

When compared against the single-switch noise, below 2 MHz and above 5 MHz regions the noise is reduced on an average of 20 dB and about 13 dB in between 2-5 MHz. It is worth noting that the best noise reduction of 32.5 dB at frequencies 1.6 MHz is obtained with this technique. Therefore, it is clear that the proposed hybrid balance technique offers better conducted CM noise reduction than the single-

switch converter within the conducted emission band (150 kHz – 30 MHz).

8. Conclusions

The typical single MOSFET converter has three dominating factors (DC source, TP, and load), which cause the circuit imbalance. The unbalanced characteristics of the single-switch converter can be improved using the hybrid balance scheme where two-switch (active balance) converter plus capacitors are in center-tap arrangement (passive balance) at both DC source and load. With this scheme, the CM noise caused by imbalance effects will be cancelled at the frame ground (FG). The measurements of CMRRs (degree of circuit balance) for single-switch converter are 5.29 dB, for two-switch converter of 12.46 dB, and 41.36 dB for the hybrid balance. Between the single and hybrid schemes, the hybrid realizes about 36.07 dB of greater balance than the single-switch circuit. Hence, the hybrid balance technique is a very effective way to improve the balance and thus reduces the conducted CM noise (EMI emissions) in the power MOSFET switching system.

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