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Tunable Gm-C Floating Capacitance Multiplier

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Abstract—This paper presents a realization of Gm-C floating capacitance multiplier. It employs MOS transistors as transconductors and only one grounded capacitor. The circuit offers the attractive features of simple configuration, electronically tunable capacitance multiplication factor, low sensitivities to variation of active and passive elements and suitability for integrated circuit implementation. The parasitic effects of the transconductors on the proposed floating capacitance multiplier are investigated. The performance of the proposed circuit is demonstrated on second-order band-pass filter. The PSPICE simulations using TSMC 0.18 μm CMOS process parameter are also given to confirm the theoretical analysis.

Keywords— floating capacitance multiplier; grounded capacitor; transconductor; high-pass filter; band-pass filter

I. INTRODUCTION

A capacitor is an important element in circuit design and can be used in many blocks such as filters, oscillators, and impedance matching circuitry. In modern integrated circuit design, the fabrication of high-valued integrated capacitors is a major problem, owing to their large occupation of silicon area. A possible solution of the problem is represented using the capacitance multiplication method. Thus, capacitance multipliers have received considerable attention. This attention is widely focused on the capacitance multiplication employing several active building blocks such as second generation current conveyors (CCII) [1-2, 4, 5], operational amplifier (OPAMP) and operational transconductance amplifiers (OTAs) [3], current-controlled differential difference current conveyors (CCDDCCs) [6], voltage differencing buffered amplifier (VDBA) [7] and Current amplifier and DUA [8]. The circuit of [1-5] provides a grounded capacitance multiplier. However, a floating capacitance multiplier can offer wider applications than a grounded capacitance multiplier. The floating capacitance multipliers have been reported [3-6]. The circuit of [5] requires two OTAs, an OPAMP, a voltage buffer, and an ungrounded capacitor. The circuit enjoys the attractive feature of electronic tuning of capacitance multiplication factor. But it might have the bandwidth and the slew rating problems because of the OPAMP used and not attractive for integrated circuit implementation. Since the CCII offers several advantages such as larger dynamic range, wider bandwidth, and greater linearity over voltage-mode counterpart like OPAMP [9-10], it is very attractive for realization of the floating capacitance multiplier. The CCII-based floating

capacitance multipliers have been proposed [4-5]. However, the floating capacitance multipliers do not offer electronic tunability. The new floating capacitance multiplier recently reported in [6] employs three CCDDCCs and a grounded capacitor. It provides the attractive features of electronic tuning of the capacitance multiplication factor and suitable for integration. Unfortunately, the circuit employs many transistors and consequently suffers from high power consumption and large area occupation in integrated circuit fabrication. Reference [7] has been proposed the tunable capacitance multiplier with a VDBA. It consists of one floating capacitor and an external resistor. Recently, [8] is presented the floating capacitance multiplier. However, the floating capacitor is employed in the same as [7].

In this paper, a new floating capacitance multiplier based on Gm-C is presented. It consists of sixteen MOS transistors as transconductors and a grounded capacitor. The multiplication factor of the proposed capacitance multiplier can be tuned electronically by current bias of the transconductor. Since the circuit employs the grounded capacitor and no external resistor, it is suitable for integrated circuit implementation. PSPICE simulation results of the proposed circuit and its application show good agreement with the theoretical analysis.

II. CIRCUIT DESCRIPTION

A. Basic Circuit Configuration

The basic circuit of the proposed floating capacitance multiplier is shown in Fig. 1(a), consisting of five voltage-controlled current sources and only one grounded capacitor. In Fig. 1(b), its equivalent circuit is shown. The current and voltage relations of node A and node B produce

$$V_A = \frac{sk_1C_1}{k_2k_3}(V_1 - V_2). \quad (1)$$

Setting $k_4 = k_5$ gives

$$I_1 = k_4V_A, \quad (2)$$

and

$$I_2 = -k_4V_A. \quad (3)$$

Substituting (1) into (2) and (3) yields the following short circuit admittance matrix

$$[Y_1] = \frac{sk_1k_4C_1}{k_2k_3} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}, \quad (4)$$

where k_i is the transconductance gain of the i^{th} voltage-controlled current source. From (4), the basic circuit realizes a floating capacitance multiplier with the equivalent capacitance as

$$C_{eq} = \frac{k_1 k_4}{k_2 k_3} C_1. \quad (5)$$

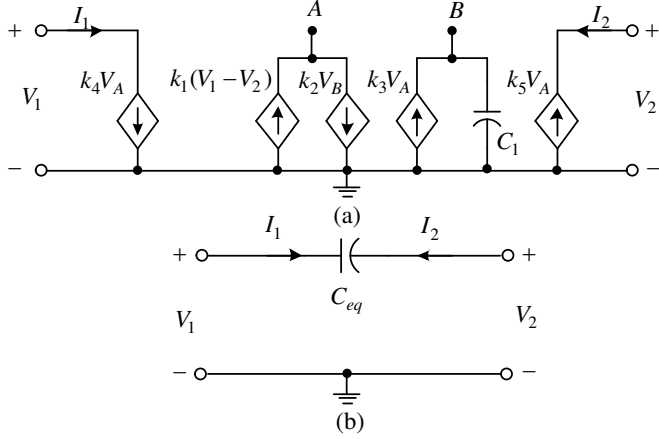


Fig. 1. (a) Proposed basic circuit, (b) its equivalent circuit.

It is noticed that the equivalent capacitance value is tuned by changing the transconductance gains. The proposed floating capacitance multiplier based on G_m -C is described in the following section.

B. Proposed Floating Capacitance Multiplier

As previously discussed in the last section, the proposed floating capacitance multiplier employs the transconductors. Thus, the significant properties of the transconductor are briefly reviewed. A simple transconductor using four CMOS transistors and two bias current sources is shown in Fig. 2(a) [11]. It is assumed that all transistors operate in the saturation region and have the same transconductance parameters. The equivalent circuit of the transconductor is illustrated in Fig. 2(b). The output currents of the transconductor yield

$$I_P = g_m V_I, \quad (6)$$

and

$$I_N = -g_m V_I, \quad (7)$$

where g_m is the transconductance value of the NMOS transistor and defined by

$$g_m = (\mu_n C_{ox} \frac{W}{L} I_B)^{\frac{1}{2}}, \quad (8)$$

where μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, W/L is the aspect ratio of the transistor and I_B is the bias current of the transconductor. Since the voltage-controlled current sources of the basic circuit as shown in Fig. 1(a) replaced by the transconductor of Fig. 2(a), the realization of the proposed floating capacitance multiplier is shown in Fig. 3.

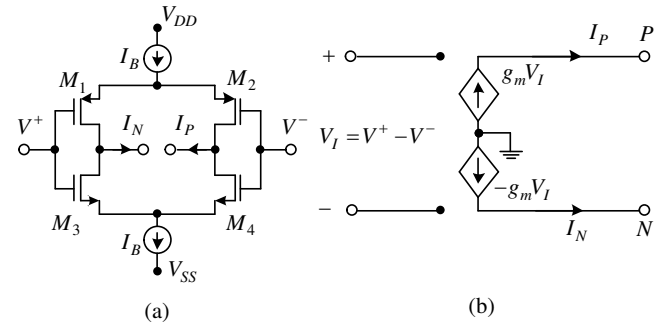


Fig. 2. (a) Simple transconductor, (b) its equivalent circuit.

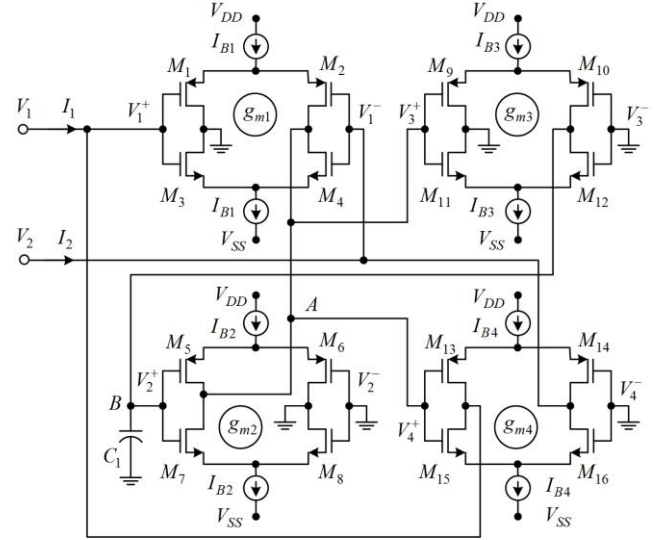


Fig. 3. Proposed floating capacitance multiplier.

This proposed circuit employs four transconductors and only one grounded capacitor. Routine analysis of the circuit yields the following admittance matrix

$$[Y_2] = \frac{sg_{m1}g_{m4}C_1}{g_{m2}g_{m3}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}, \quad (9)$$

where g_{mi} is the transconductance value of the i^{th} transconductor. Comparison of (4) and (9) results $k_i = g_{mi}$, then the equivalent capacitance of the proposed circuit can be expressed as

$$C_{eq} = \frac{g_{m1}g_{m4}}{g_{m2}g_{m3}} C_1. \quad (10)$$

From (10), the capacitance multiplication factor is given by

$$K = \frac{g_{m1}g_{m4}}{g_{m2}g_{m3}}. \quad (11)$$

Thus, the multiplication factor, K , can be electronically adjusted by changing the bias currents of the transconductors. The sensitivities of the equivalent capacitance with respect to active and passive elements yield the acceptably low values as follows: $S_{g_{m1}}^{C_{eq}} = -S_{g_{m2}}^{C_{eq}} = -S_{g_{m3}}^{C_{eq}} = S_{g_{m4}}^{C_{eq}} = S_{C_1}^{C_{eq}} = 1$. (12)

C. High Frequency Consideration

From (9), the short circuit admittance matrix of the proposed circuit has been realized by considering the ideal description of the transconductor. For high frequency application, the parasitic elements of the transconductor affect the frequency response of the proposed circuit. The equivalent circuit of the transconductor with the parasitic elements is shown in Fig. 4. It is shown that input terminal exhibits low-value capacitances C_{I+} and C_{I-} and output terminals exhibit low-value capacitances C_P and C_N with low-value conductances G_P and G_N , respectively.

Considering the above parasitic elements, routine analysis of the proposed circuit as shown in Fig. 3 gives the following short circuit admittance matrix

$$[Y_3] = \begin{bmatrix} \frac{1}{Z_{X1} // Z_T} & -\frac{1}{Z_T} \\ \frac{1}{Z_T} & \frac{1}{Z_{X2} // Z_T} \end{bmatrix}, \quad (13)$$

where $Z_{X1} = \frac{1}{s(C_{I1+} + C_{N4}) + G_{N4}}$, $Z_{X2} = \frac{1}{s(C_{I1-} + C_{P4}) + G_{P4}}$ and $Z_T = \frac{g_{m2}g_{m3} + \Delta_T[s(C_1 + C_{I2+} + C_{P3}) + G_{P3}]}{g_{m1}g_{m4}[s(C_1 + C_{I2+} + C_{P3}) + G_{P3}]}$, where Δ_T is given by $\Delta_T = s(C_{P1} + C_{N2} + C_{I3+} + C_{I4+}) + G_{P1} + G_{N2}$.

Note that the terms of impedances $1/[s(C_{I1+} + C_{N4}) + G_{N4}]$ and $1/[s(C_{I1-} + C_{P4}) + G_{P4}]$ are effective at very high frequencies. It is also high frequency limitation depending on the passive element selection. The limitation at high frequencies is found to be

$$\omega \ll \min \left\{ \frac{G_{P3}}{C_1 + C_{I2+} + C_{P3}}, \frac{G_{N4}}{C_{I1+} + C_{N4}}, \frac{G_{P4}}{C_{I1-} + C_{P4}} \right\}. \quad (14)$$

It is seen from (14) that C_1 is chosen as small as possible to increase the high frequency performance of the proposed circuit.

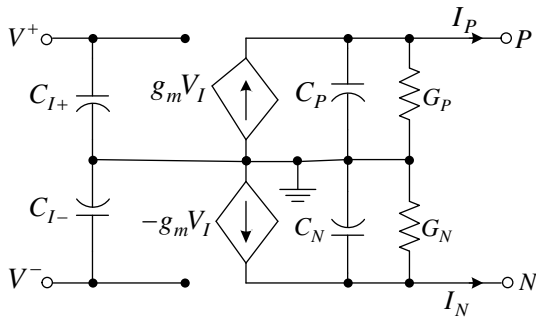


Fig. 4. The equivalent circuit with parasitic elements of the transconductor.

III. APPLICATION EXAMPLES

A. Second-order High-pass and Band-pass Filters

To illustrate an application of the proposed floating capacitance multiplier of Fig. 3, it is used to implement an active capacitor in a second-order band-pass filter (BPF) as shown in Fig. 5 [12].

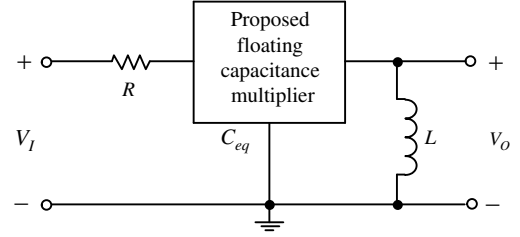


Fig. 5. Second-order band-pass filter.

The transfer function of the filter can be expressed as

$$H_{BPF}(s) = \frac{s \frac{g_{m2}g_{m3}}{g_{m1}g_{m4}RC_1}}{s^2 + s \frac{g_{m2}g_{m3}}{g_{m1}g_{m4}RC_1} + \frac{g_{m2}g_{m3}}{g_{m1}g_{m4}LC_1}} \quad (15)$$

The center or resonant frequency ω_0 , quality factor Q and bandwidth BW of the BPF can be given as

$$\omega_0 = \sqrt{\frac{g_{m2}g_{m3}}{g_{m1}g_{m4}LC_1}}, \quad Q = R \sqrt{\frac{g_{m1}g_{m4}C_1}{g_{m2}g_{m3}L}}, \quad \text{and } BW = \frac{g_{m2}g_{m3}}{g_{m1}g_{m4}RC_1}.$$

The sensitivities of the filter parameters are found as

$$-S_{g_{m1}}^{a_b} = S_{g_{m2}}^{a_b} = S_{g_{m3}}^{a_b} = -S_{g_{m4}}^{a_b} = -S_L^{a_b} = -S_{C_1}^{a_b} = \frac{1}{2}, \quad (16)$$

$$S_{g_{m1}}^Q = -S_{g_{m2}}^Q = -S_{g_{m3}}^Q = S_{g_{m4}}^Q = -S_L^Q = S_{C_1}^Q = 2S_R^Q = \frac{1}{2}, \quad (17)$$

and

$$-S_{g_{m1}}^{BW} = S_{g_{m2}}^{BW} = S_{g_{m3}}^{BW} = -S_{g_{m4}}^{BW} = -S_R^{BW} = -S_{C_1}^{BW} = 1, \quad (18)$$

which are all no more than unity in absolute value. Thus, the proposed circuit exhibits an attractive sensitivity performance.

IV. SIMULATION RESULTS

To verify the performance of the proposed floating capacitance multiplier as shown in Fig.3, it has been simulated using PSPICE program based BSIM3 level 7 transistor models for the TSMC 0.18 μ m CMOS process with ± 0.9 V supply voltage. The parameters of the NMOS and the PMOS transistors are listed in [13] available from MOSIS. The aspect ratios (W/L) of CMOS transistors are assumed of 3.6 μ m/0.54 μ m for NMOS and 9 μ m/0.54 μ m for PMOS. Fig. 6 shows impedance values relative to frequency of the proposed circuit with different bias current of the first transconductor, I_{B1} . Similarly, the floating capacitances were simulated by adjusting I_{B1} . The results of the capacitances are shown in Fig.

7. They confirm that the simulated capacitance can be adjusted by control the bias currents of the transconductors.

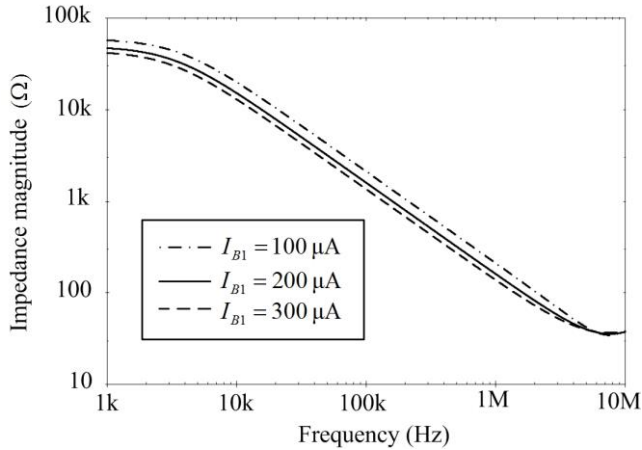


Fig. 6. Impedance characteristics of the proposed circuit for different bias current.

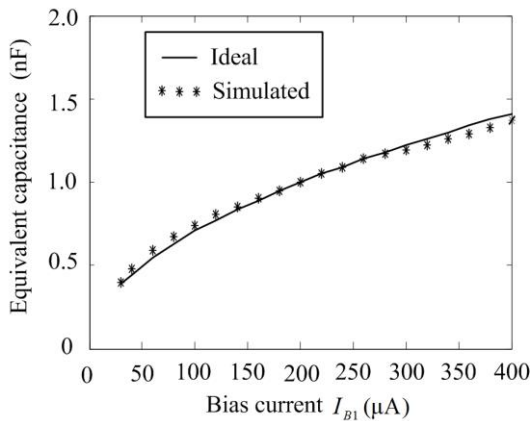


Fig. 7. Variation of the simulated capacitances versus ideal ones as the bias current is varied.

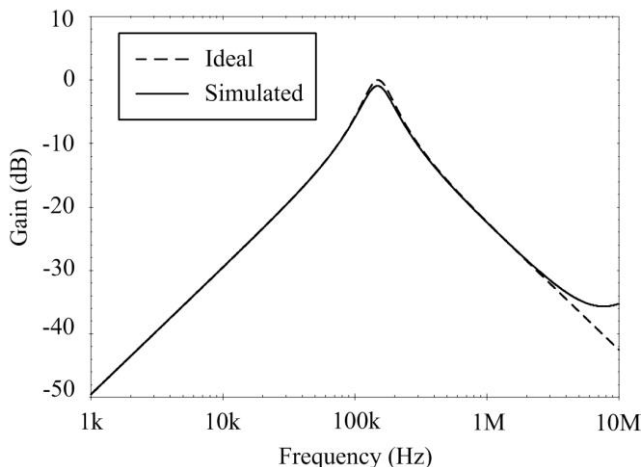


Fig. 8. Simulated and ideal frequency responses of the BPF as shown in Fig. 6.

For the application example, Fig. 8 shows the simulated and ideal frequency responses of the BPF as shown in Fig. 5. The filter is designed on the 1nF proposed floating capacitance multiplier of Fig. 3 and passive elements of $R = 2.13 \text{ k}\Omega$ and $L = 1.13 \text{ mH}$, resulting in the center frequency of $f_0 = 150 \text{ kHz}$, a quality factor of $Q = 2$, and a bandwidth of $BW = 469.48 \text{ kHz}$. The proposed capacitance multiplier is set as follows: $I_{B1} = I_{B4} = 200 \text{ }\mu\text{A}$, $I_{B2} = I_{B3} = 20 \text{ }\mu\text{A}$, and $C_l = 100 \text{ pF}$. It should be noticed that the simulated result of the filter very closely approximates the theoretical one.

V. CONCLUSION

The floating capacitance multiplier-based G_m -C is proposed in this paper. Its configuration is very simple. It employs only a grounded capacitor without another passive element, so the proposed capacitive multiplier is particularly attractive for IC implementation. Moreover, the multiplication factor of the proposed circuit can be electronically tuned by changing the bias current of the transistor. The simulation results of the proposed capacitance multiplier and its application show good agreement with the theoretical predictions.

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